WIRELESS USER TERMINAL AND SYSTEM HAVING SIGNAL CLIPPING CIRCUIT FOR SWITCHED CAPACITOR SIGMA DELTA ANALOG TO DIGITAL CONVERTERS

Field of the Invention

This invention relates generally to the field of electronic systems and, in particular, to a wireless user terminal and system having signal clipping circuits for switched capacitor sigma delta analog-to-digital converters included within audio codec systems.

Background of the Invention

The codifier/decodifier (CODEC) is the algorithm that handles the coding and decoding of audio signals within an electronic system. Specifically, an audio CODEC is a custom mixed-signal core providing analog-to-digital (A/D) and digital-to-analog (D/A) conversion. A simple serial interface is used to exchange digital data (D/A input and A/D output) between the application specific integrated circuit (ASIC) and CODEC core. Prior art CODEC features delta-sigma A/D and D/A oversampled converters and low power dissipation.

A typical uplink channel for a mobile phone voiceband or audio CODEC includes a microphone, amplifier, sigma-delta analog-to-digital converter (ADC) and a digital filter coupled together on one chip. This first chip couples to a digital signal processor for processing the digital signal received. Another chip includes a radio frequency (RF) modulator which is coupled to a last component that includes a RF power amplifier. The signal is transmitted over an antenna to a downlink channel for the mobile phone voiceband CODEC.

Initially, the audio CODEC receives an analog voice signal through the microphone and converts it to a digital signal. The digital signal is forwarded to a digital signal processor for processing. This signal is transmitted to a receiver. In the receiver, the digital signal is processed through the digital signal processor and forwarded to a D/A converter. The analog signal is fed to a speaker.

In most prior art CODECs, the sigma-delta ADC is scaled for a maximum output corresponding to the +3dbm0 code of the pulse code modulation (PCM) data. The analog signal corresponding to this digital upscale value is far less than the maximum allowable dynamic range, which usually is limited by the supply range. This fact could potentially overload the A/D and consequently the digital filter. An FCC test, mandatory in the U.S., falls under this category. Once the digital filter overloads, internal clipping mechanisms prevent wrap around of the digital signal, thus creating a digital representation of a trapezoidal signal that contains harmonics with sufficient power to increase the FM modulation depth.

First and second order sigma delta analog modulators are inherently stable under large input level variations. Higher order modulators, however, can become unstable during the overload condition. Clipping the input signal to a pre-determined safe operation level, prevents the modulator from going unstable, without having the need to recover stability after the overloading condition is removed. In other cases, even inherently stable sigma-delta structures have to be protected by a clipping mechanism to prevent post digital filtering from generation of a rail-to-rail digital representation of a quasi-square wave which can over-modulate the RF channel in a typical transmit CODEC channel for wireless applications.

Several implementations have been proposed to solve this problem. Most of them deal with clipping the signal in a previous analog amplifier stage. One solution is provided in U.S. Patent Application 09/351,610, which discloses a multiplexer amplifier having an analog output signal, a sigma-delta ADC having an input coupled to the analog

output signal and a clipping circuit coupled to the input of the ADC for clipping the analog output signal. While this analog solution avoids saturation and provides an effective clipping mechanism to prevent wrap around of the digital signal, it is prone to overshoot and settling issues.

In present systems, however, the signal is fed to the A/D directly from external sources, such as a microphone or an RF mixer. Accordingly, many audio CODECs no longer include the microphone and amplifier. Thus, there is a need for a wireless user terminal and system that incorporate a sigma-delta analog-to-digital converter (ADC) that is free of overshoot and settling issues.

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Summary of the Invention

A wireless user terminal and system that implement a mixed signal CODEC including an improved sigma-delta ADC limits input signals into a switched capacitor configuration and avoids adding circuit overhead in the signal path. Additionally, the improved sigma-delta ADC substantially reduces overshoot and settling problems common in user terminals. This improved sigma-delta ADC, having an input signal and an output signal, includes a switch, a clipping circuit, and a sigma-delta ADC. It solves the clipping signal problem in wireless user terminals by limiting the signal right at the input of the sigma-delta ADC. The clipping circuit couples to the switch and the sigma-delta ADC for switching the voltage applied to the sigma-delta ADC between the input signal and at least one threshold voltage. When the input signal goes above a prescribed upper threshold, the fixed threshold voltage is applied to the sigma-delta ADC, which converts fixed threshold voltage into a digital signal. Moreover, when the input signal goes below that prescribed threshold, the incoming signal is applied to the sigma-delta ADC, which converts the incoming signal. In the alternative, when the input signal goes below a prescribed lower threshold, the fixed threshold voltage is applied to the sigma-delta ADC, which converts fixed threshold voltage. Furthermore, when the input signal

goes above that prescribed threshold, the incoming signal is applied to the sigma-delta ADC, which converts the incoming signal. Given this solution, minimum power and area overhead exist.

Brief Description of the Drawings

For a more complete understanding of the present invention and the advantages thereof, reference is now made to the following description taken in conjunction with the accompanying drawings in which like reference numbers indicate like features and wherein:

Figure 1 is a schematic of a known simplified input stage of a sigma delta modulator;

Figure 2 is a schematic of a signal clipping circuit in accordance with the present invention;

Figure 3a is a diagram of the input voltage applied with respect to time; and

Figure 3b is a diagram of the clipped input voltage in accordance with the present invention.

Figure 4 illustrates a communications system that implements the signal clipping circuit of one embodiment of the present invention;

Figure 5 illustrates a block diagram of a wireless user terminal implemented in an embodiment of the present invention;

Figure 6 illustrates a wireless user terminal block diagram that implements the signal clipping circuit according to an embodiment of the present invention;

Figure 7 illustrates a wireless user terminal receiver block diagram that implements the signal clipping circuit according to an embodiment of the present invention;

Figure 8 illustrates the transmitted spectra for TDMA (GSM) and CDMA (IS-95) systems; and

Figure 9 illustrates a spectral definition of 2G and 3G cellular regulations.

Detailed Description of Preferred Embodiments

A circuit is presented here, that clips the incoming signal to predetermined levels without disturbing the signal path and adding little overhead to the power and area requirements. In Figure 1, analog clipping circuits 40 and 42 are coupled to the differential inputs of the sigma-delta A/D 26, to avoid overdriving the sigma-delta A/D 26. The analog clipping circuits 40 and 42 add minimum overhead in area and power. For the preferred embodiment, the maximum allowable dynamic range at the input of the sigma delta A/D 26 is a minimum of 0.625 volts and a maximum 2.375 volts. The fully differential signal is 3.5 volts (+1.75 volts to –1.75 volts). Each single ended signal is clipped at a low of 0.625 volts (V_{RL}) and a high of 2.375 volts (V_{RH}). This clipping problem solution adds a pre-amp to the signal path. The amplifier then, has to perform better than the noise specification of the channel which implies high current consumption and silicon area utilization. This solution adds a constraint to the external driving source since now the input to the chip is not capacitively coupled anymore but rather has low resistance.

A voiceband CODEC 18 having an improved sigma-delta A/D converter in accordance with the present invention is shown in Figure 2. The incoming signal v_{in} is connected to the comparators C_p 24 and C_n 22 (which can be designed for very low

current since speed and offset are not a primary concern), as well. Threshold voltages, V_p and V_n (which can be generated from the bandgap or derived from the supply voltage through a resistor/diode division), are coupled to comparators, C_p 24 and C_n 22, respectively. The incoming signal is sensed by comparators C_p and C_n, comparing the incoming signal with voltages V_p and V_n. Comparators C_p and C_n are connected to switches, sw_p and sw_n, respectively for switching in voltage levels, V_p and V_n, respectively. All three switches, sw_1, sw_p and sw_n, couple to a sigma-delta ADC 34. Switch sw_1 couples to receive the incoming signal v_{in}.

In operation, when incoming signal v_{in} rises above the threshold voltage V_p, switch sw_1 opens and comparator C_p turns on, closing switch sw_p. Accordingly, the fixed voltage V_p is supplied to the sigma delta ADC 34. When the value of the signal goes below the threshold voltage, comparator C_p shuts off, opening switch sw_p. Simultaneously, switch sw_1 closes and incoming signal v_{in} is supplied directly to sigma-DAC 34.

When incoming signal v_{in} goes below threshold voltage V_n, switch sw_1 opens and comparator C_n turns on, closing switch sw_n. Accordingly, the fixed voltage V_n is supplied to the sigma delta ADC 34. When the value of signal v_{in} rises above the threshold voltage V_n, the comparator C_n shuts off, opening switch sw_n. Simultaneously, switch sw_1 closes and incoming signal v_{in} is supplied directly to the sigma delta ADC.

Figure 3a displays the input signal v_{in}, while Figure 3b shows the clipped input signal v_{clip} seen by the sigma-delta ADC 34. As shown in Figure 3b, when incoming signal v_{in} rises above the threshold voltage V_p, switch sw_1 opens and comparator C_p turns on, closing switch sw_p. As a result, the voltage v_{clip} is equal to the threshold voltage V_p. When the value of the signal v_{in} goes below the threshold voltage V_p, the comparator C_p shuts off, opening switch sw_p. Switch sw_1 closes and, as a result, voltage v_{clip} equals the incoming signal v_{in}. When the incoming signal v_{in} goes below threshold voltage V_n,

switch sw_1 opens and the comparator C_n turns on, closing switch sw_n. Accordingly, voltage v_{clip} equals the fixed voltage V_n.

The signal clipping circuit for switched capacitor sigma delta analog-to-digital converter (ADC) of the present invention can be used in a variety of telecommunication and other applications. Conveniently, the signal clipping circuit for improved sigma delta analog-to-digital converters can be implemented in wireless user terminals and base stations operating according to international standards, such as for example CDMA (Code Division Multiple Access) and GSM (Global System for Mobile Communication).

Figure 4 illustrates a wireless communication system in which the signal clipping circuit for improved sigma delta analog-to-digital converters of the present invention may be implemented. Wireless communication system 40 comprises a wireless user terminal (a cellular handset being illustrated) 42 that communicates with a base station (a cellular base station being illustrated) 44 over an uplink channel 46 and downlink channel 48. The base station and the wireless user terminal unit operate in a similar manner.

Cellular communication in system 40 can be facilitated in Time Domain Duplex (TDD) or in Frequency Domain Duplex (FDD). In Time Domain Duplex (TDD) the communication between wireless user terminal 42 and base station 44 is on a single channel. Much like a walky-talky, the channel is shared in time by the mobile station transmitter and the base station transmitter. A time slot is dedicated to the uplink and another timeslot is dedicated to a downlink. The relative length of the uplink and downlink time slots can be adjusted to accommodate asymmetric data traffic. If it is found that downlink data traffic is on average twice that of uplink, then the downlink time slot is twice as long as the uplink time slot. In Frequency Domain Duplex (FDD) the wireless user terminal 42 and the base station 44 communicate over a pair of radio frequencies. The lower frequency is the uplink during which the mobile station sends information to the base station. Both uplink and downlink are each composed of a signal source, a transmitter, the propagation path, a receiver and a method of presenting the

information. Both wireless user terminal and base station embody the invention with transmitters, which convert digital data to analog signals at high speed and with high resolution. The base station could convert the entire multi-carrier downlink signal to analog for use in a single RF transmitter. The wireless user terminal is explained in the following.

Figure 5 presents a top-level block diagram 50 of the wireless user terminal 42. In wireless user terminal 42, radio frequency (RF) signals are received and transmitted by the RF section 52. In the embodiment illustrated, RF section 52 comprises a duplexer 76 coupling an antenna 78 to a receiver 68 and a power amplifier 74. A modulator 72 is coupled to power amplifier 74 and to a synthesizer 70. Synthesizer 70 is further coupled to receiver 68. RF section 52 is further coupled to an analog baseband 54. In the embodiment illustrated, analog baseband 54 comprises an RF interface 56 and an audio interface 58. A speaker 88 and a microphone 90 are coupled to audio interface 58. RF interface 56 is coupled to both receiver 68 and modulator 72 of RF section 52. The analog RF interface 56 includes I and Q analog-to-digital converters (ADCs), according to the present invention, and digital-to-analog converters (DACs), for conversion between the analog and digital domains. Audio interface 58 may also include I and Q analog-to-digital converters (ADCs), according to an embodiment of the present invention, and digital-to-analog converters (DACs), for conversion between the digital and analog domains. Analog baseband 54 is further coupled to a digital baseband 60.

In the illustrated embodiment, digital baseband 60 comprises three elements: digital signal processor (DSP) 62, microcontroller unit (MCU) 64 and application specific integrated circuit (ASIC) 66. DSP 62 couples audio interface 54 to RF interface 56 and to microcontroller unit (MCU) 64. Digital signal processor (DSP) 62 and microcontroller unit (MCU) 64 are further coupled to ASIC backplane 66. Microcontroller unit (MCU) 64 is further coupled to a user interface 80, which comprises at least a user display 82 and a keyboard 84 (an optional SIM card 86 is also disclosed).

The digital signal processor (DSP) 62, provides programmable speech coding and decoding (vocoder), channel coding and decoding, equalization, demodulation and encryption. The microcontroller unit (MCU) handles level 2 & 3 protocol, radio resource management, short message services, man-machine interface and the real-time operating system. The ASIC backplane 66 performs all chip-rate processing. While top level diagram 50 illustrates RF section 52, analog baseband 54 and digital baseband 60 as being separate packages or chips, the invention contemplates substitution of any of the above with an equivalent function, such as an RF function, and/or an analog baseband function and/or a digital baseband function. The functions will remain the same even if the actual implementation varies. The invention further contemplates that RF section 52, analog baseband 54 and digital baseband 60 may be selectively combined and/or integrated into one or two packages or chips.

An uplink voice processing chain 46 for a wireless user terminal 42 is illustrated in Figure 6. This channel includes a CODEC 100 coupling a microphone 90 to a vocoder 98, a baseband modulator 96 coupling vocoder 98 to a digital-to-analog converter 92 at high speed and high resolution. An RF transmitter 94 (part of RF section 52) couples an antenna 78 to digital-to-analog converter 92. Within RF transmitter 94, modulator 72 is implemented as two RF mixers, I and Q driven by the synthesizer, implemented as an RF local oscillator. RF transmitter CODEC 100 includes an audio amplifier (not shown), sigma-delta analog-to-digital converter (ADC) (not shown) and a digital filter (not shown) coupled together on one chip. The CODEC receives an analog voice signal through the microphone and converts it to a digital signal. While CODEC 100 is shown as being separate from digital baseband 60, it may also be internal to digital baseband 60. CODEC 100 transcodes audio signals into digital words using the algorithms contained in the VOCODER. This signal is then complex modulated, converted to analog (I&Q) and applied to the transmitter. The transmitter is complex modulated at the radio frequency assigned to the handset. It uses a power amplifier coupled to the antenna 78 to transmit the digital signal, effectively communicating the (digital) voice information to the base station receiver.

A downlink voice channel 48 for wireless user terminal 42 is illustrated in Figure 7. This channel includes an RF receiver 102 (part of RF section 52) coupling antenna 78 to an analog-to-digital converter (ADC) 104, according to the invention, a vocoder 98 coupling a demodulator 96 to a CODEC 100, and a speaker 88 coupled to CODEC 100. While CODEC 100 is shown as being separate from digital baseband 60, it may also be internal to digital baseband 60. CODEC 100 transcodes the digital words into analog signals using the algorithms contained in the VOCODER. CODEC 100 includes a digital filter, DAC and audio amplifier coupled together on one chip. The RF receiver uses an AGC circuit which varies the IF amplifier gain as a function of the received signal. The goal is to present the analog-to-digital converters (ADCs) with a full-scale analog signal without distortion and with minimal noise.

The band structure of the cellular system in which the communication system of the present invention operates is composed of tightly packed RF carriers with very high spectral density. As illustrated in Figure 8, the world's most widely deployed TDMA system is GSM, where the GMSK-modulated carriers are placed on a 200-Khz raster 106 with adjacent channel signal interference suppressed to -30dBc at the first adjacent channel and -60dBc at the second. The 2-G CDMA system used in America (IS-95) uses QPSK-modulated (at 1.2288 Msps) carriers spaced at 1.25 Mhz 108 with very little guard band. Each carrier can be modulated with up to 32 Walsh codes, which are used to separate the users.

Figure 9 illustrates the spectral definition of the 2G and 3G cellular regulations. The base station transmitter operates on the upper frequency band. For example, in Europe the base station receives from 1900 to 1980 Mhz and transmits from 2110 to 2170 Mhz.

The signal analog-to-digital converter of the present invention can be use in other applications, such as data communication systems, hard disk drives, cd players, video

displays, and any other application where there is a large amount of data that must be converted quickly.

Those skilled in the art to which the invention relates will appreciate that various substitutions, modifications and additions can be made to the described embodiments, without departing from the spirit and scope of the invention as defined by the claims.